AIKO ELECTRO

AKSDM0470
Quasi Resonant Primary Feedback CC/CV PWM Power Supply Controller

Features:
- Built in 700V power MOS
- Efficient quasi resonant primary side feedback regulation (QR-PSR) control
- Audio noise removal function± 4% adjustment rate for CC and CV
- Optimized dynamic response
- Low standby power consumption<75mW
- Programmable cable voltage drop compensation (CDC) in CV mode
- Built in line voltage and load constant current compensation
- Pulse Leading Edge Blanking (LEB)
- Protection function:
  - ➢ Load short circuit protection (SLP) with cycle by cycle current limitation
  - ➢ FB pin open circuit/short circuit protection
  - ➢ VDD overvoltage/undervoltage/clamp protection
  - ➢ Overheat protection (OTP)
- DIP7 packaging

Applications:
- Mobile phone battery charger
- AC/DC power adapter
- LED lighting power supply

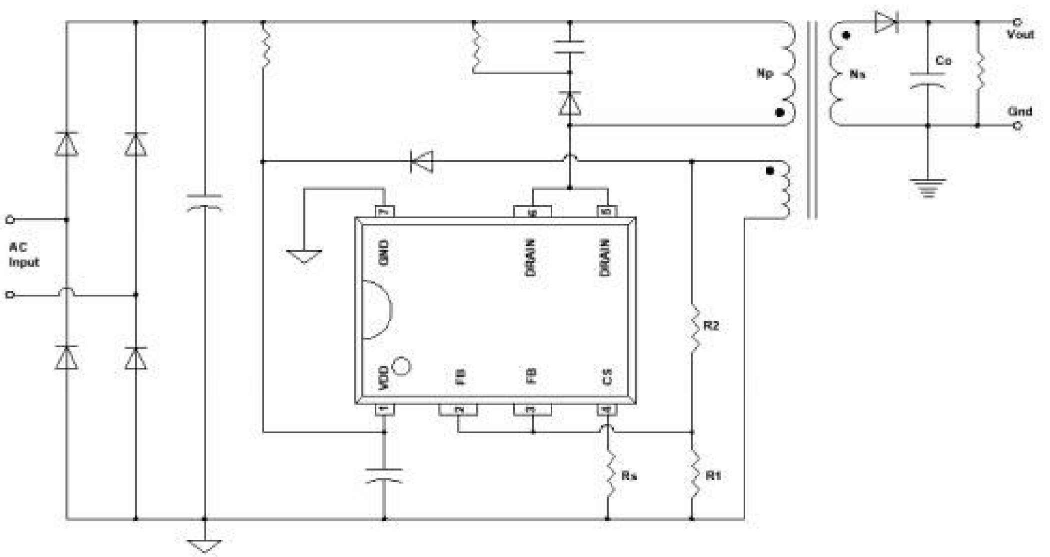
Introduction:
AKSDM0470 is a high-performance quasi resonant primary feedback controller applied to offline low-power AC/DC switching power supplies, providing a cost-effective solution for low-cost switching power supply systems,It can provide high-precision CC/CV control, and is suitable for applications such as chargers, adapters, and built-in power supplies. In constant voltage CV mode, using quasi resonance and multi technology to improve efficiency and eliminate audio noise, the system can meet the 6-level energy efficiency standard, and the adjustable output line compensation function enables the system to achieve better load adjustment rate; In constant current CC mode, the output current and power can be adjusted through CS resistors.

AKSDM0470 provides comprehensive protections: undervoltage lockout (UVLO), VDD overvoltage protection (VDD0VP), cycle by cycle overcurrent protection (OCP), short circuit protection (SLP), FB pin open/short circuit protection, VDD clamping, overheating protection (OTP), and other protections.

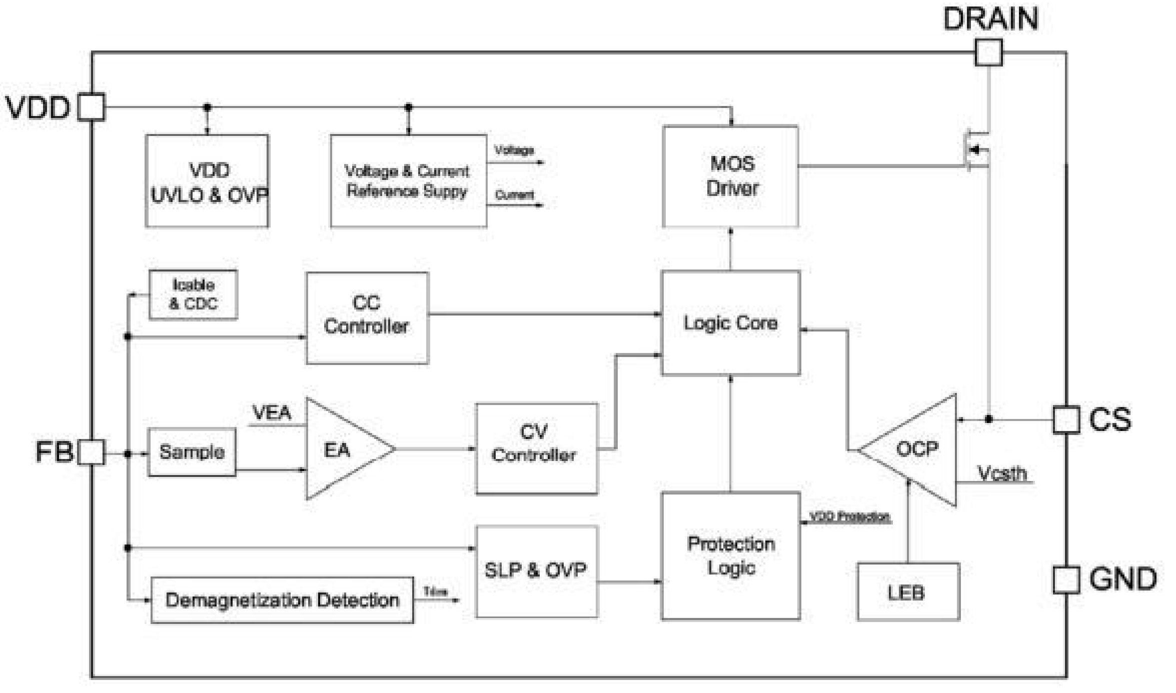
Outline / Packaging

PRODUCT	OUTLINE	PACKAGE
SSDM0470	DIP-7	

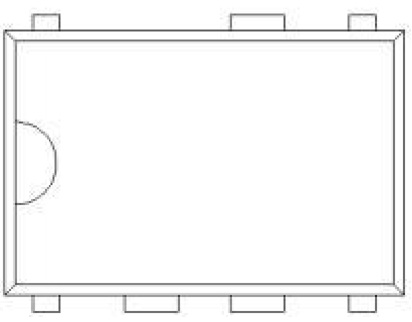
Typical Application



Interior Circuit



Pin Function Instruction

DIP-7	Pin Num	Pin Name	I/O Description
	1	VDD	The power pins of the IC
	2/3	FB	System feedback pins, based on the flyback power supply of the auxiliary winding, in CC mode or CV
	4	CS	The input terminal of current detection.
	5/6	DRAIN	Built-in Power MOSFET DRAIN end
	7	GND	IC grounding pin

Limit Parameter

ITEM	VALUE	UNIT
maximum voltage resistance of high-voltage transistor	-0.3 ~ 700	V
VDD DC power supply voltage	30	V
VDD DC clamp current	10	mA
CS input voltage	-0.3 ~ 7	V
FB input voltage	-0.7 ~ 7	V
thermal resistance RθJA (℃/W)	75	℃/W
maximum junction temperature(TJmax)	150	℃
operating temperature range	-40 ~ 85	℃
storage temperature range	-65 ~ 150	℃
Pin soldering temperature (tin-soldering, 10 seconds)	260	℃
ESD，HBM (Human Body Model)	3	kV
ESD，MM(Machine Model)	250	V

Rated Operation Conditions

ITEM	VALUE	UNIT
power supply voltage VDD	7 ~ 24	V
operating temperature	-40 ~ 85	℃

Power Range

PRODUCT	175-264VAC（Adapter）	85-264VAC（Adapter）
AKSDM0470	20W	18W

Note：The maximum typical output power is tested in a closed 45 ℃ environment with sufficient heat dissipation conditions.

Electrical Characteristic Parameters (T_A = 25℃, VDD=20V, except for specifically noted conditions.

SYMBOL	ITEM	CONDITION	MIN.	TYP.	MAX.	UNIT
Power supply voltage (VDD pin)						
I_{VDD_st}	start-up current		-	3	20	uA
I_{VDD_Op}	working current		-	0.8	1.5	mA
$I_{VDD\_standby}$	standby current		-	0.5	1	mA
V_{DD_ON}	start-up voltage		15.5	16.5	17	V
V_{DD_OFF}	under voltage protection monitoring voltage		8	9	9.5	V
V_{DD_OVP}	overvoltage protection monitoring voltage		25	27.5	30	V
V_{DD_clamp}	clamping voltage	$I(V_{DD})$=7mA	32	36.5	39	V
FB PINS						
V_{FBREF}	FB threshold voltage		1.97	2	2.03	V
V_{FB_SLP}	Short circuit protection (SLP) threshold voltage		-	0.6	-	V
T_{FB_Short}	Output short circuit error prevention trigger time		-	10	-	ms
V_{FB_DEM}	Demagnetization comparator threshold		-	25	-	mV
T_{off_min}	minimum turn-off time		-	2	-	us
T_{off_max}	maximum turn-off time		-	5	-	ms
I_{cable_max}	Maximum compensation current		-	60	-	uA
T_{SW}/T_{DEM}	CC mode cycle to demagnetization time ratio		-	7/4	-	
CS PINS						
T_{LEB}	CS Input Frontier Hidden Time		-	500	-	ns
$V_{CS(max)}$	Current limiting threshold		465	480	490	mV
T_{D_OC}	Delay time for overcurrent detection		-	100	-	ns
MOS						
BV_{DSS}	Leakage breakdown voltage		700	-	-	V
R_{DS_ON}	on-state resistance		-	2.6	3.1	Ω
IC Built in overheating protection						
TSD	Over temperature protection shutdown	guarantee value design	-	155	-	℃

Application:

AKSDM0470 is a high-performance, multi-mode, and highly integrated quasi resonant primary side feedback regulation (QR-PSR) controller.

The IC is equipped with high-precision CV/CC control and multiple reliable protection functions, suitable for offline low-power power converter applications.

Start-up Operation Instruction

After the system is powered on, AKSDM0470 charges the VDD capacitor through a high-voltage starting resistor. When the VDD voltage reaches the conduction voltage (typical value of 12.5V), the IC begins to increase the working current to 1mA (typical value). The capacitor continues to provide VDD voltage until the auxiliary winding provides VDD voltage, and the system turns to normal working state.

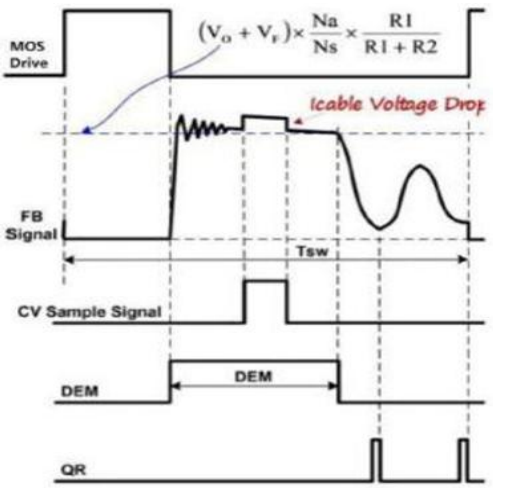
When AKSDM0470 becomes the low-frequency FM (Frequency Modulation) mode, the operating current usually decreases to 0.8mA, which helps to reduce standby power consumption.

Quasi resonant PSR constant voltage modulation (QR-CVM)

Primary feedback modulation is a method of controlling the output voltage by detecting the voltage on the auxiliary winding during the energy transfer of the secondary winding in a transformer. Picture 2 shows the working waveforms of demagnetization (DEM) and quasi resonance (QR) triggering signals during the constant voltage (CV) sampling process of AKSDM0470. In order to achieve accurate representation of the secondary output voltage on the auxiliary winding, the CV sampling signal blocks the reset of the leakage inductance. At the end of the constant voltage (CV) adoption process, the adoption/hold (S&H) circuit inside the IC captures the error signal and amplifies it through an internal error amplifier (EA). The output signal of the error amplifier (EA) is sent to the quasi resonant primary constant voltage modulation unit (QR-CVM) for constant voltage CV modulation. The QR CVM unit opens a new PWM cycle at the bottom of the voltage according to the load situation. The internal reference voltage of EA is adjusted to 2V with high precision.

During the CV sampling process, the internal variable current source flowing towards the FB pin can be used for output cable voltage drop compensation (CDC). Therefore, there is a step at the FB pin during the demagnetization process of the transformer, as shown in Picture 2. Picture 2 simultaneously expresses the "demagnetization" equation: VO and VF in the equation are the output voltage and the forward voltage of the diode; R1 and R2 are resistance dividers connected from the auxiliary winding to the FB pin, while Ns and Na are the secondary winding and auxiliary winding, respectively.

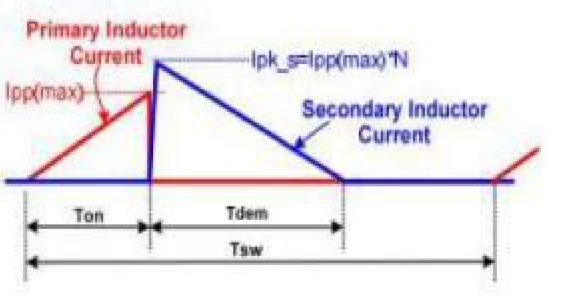
When the system enters an overload state, the output voltage drops, and the FB sampling voltage is correspondingly lower than the 2V internal reference, causing the system to automatically enter CC mode.



Picture 2

PSR Constant Current Modulation (PSR-CCM)

The timing information on the FB pin and the current information on the CS pin can accurately adjust the secondary current. The control law indicates that as the CV regulation power increases and the CC regulation approaches, the primary peak current is Ipp (max), as shown in Picture 3.



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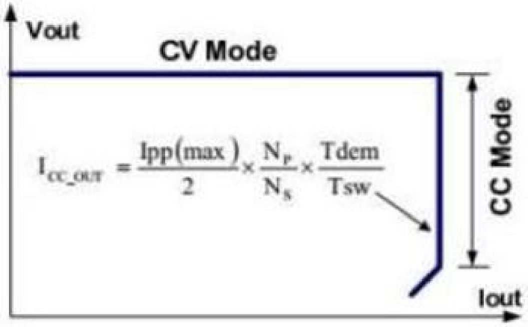
Function Description



Picture 3

Referring to Picture 3 above, the average output current IOUT of the secondary side is determined by the primary peak current IPP, transformer turn ratio, secondary demagnetization time (TDEM), and switching period (TSW). Ignoring the leakage inductance effect, the equation for the average output current is shown in Picture 3. When the average output current IOUT reaches the adjustment reference in the primary constant current modulator (PSR-CCM) module, the IC operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage equal to or lower than the voltage regulation, as long as the auxiliary winding can maintain VDD higher than VDD_ The OFF threshold is sufficient.

In AKSDM0470, the ratio between TDEM and TSW in constant current CC mode is 4/7. So the average output current can be expressed as:

$$I_{cc\_out}(\text{mA}) = \frac{2}{7} \times N \times \frac{500mV}{R_{CS}(\Omega)}$$

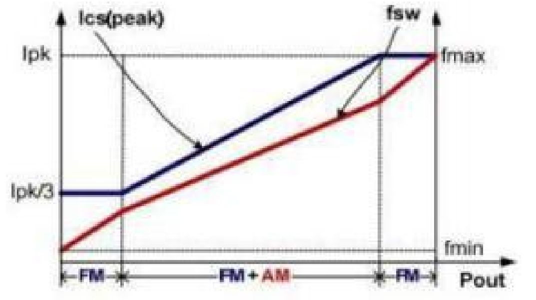
In the above equation:

N - The ratio of turns between the primary and secondary windings of a transformer;

RCS -- The current sampling resistance between the IC CS pin and GND.

Multiple Modes of Constant Voltage Control

In order to meet the strict requirements of average system efficiency and no-load power consumption, AKSDM0470 adopts a mixture of frequency modulation (FM) and amplitude modulation (AM), as shown in Picture 4. Under full load, the system operates in FM mode. Under normal light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system approaches zero load, the IC enters FM mode again to reduce standby power consumption. In this way, the no-load loss will be less than 75mA.



Programmable Cable Voltage Drop Compensation in CV Mode

In smartphone charger applications, the battery is always connected to the adapter through a data cable, which may cause a voltage drop of several percent in the charger's output voltage on the battery. In AKSDM0470, an internal current source (modulated by the CDC module, as shown in Picture 5) flows into the resistive voltage divider, generating a bias voltage at the FB pin.

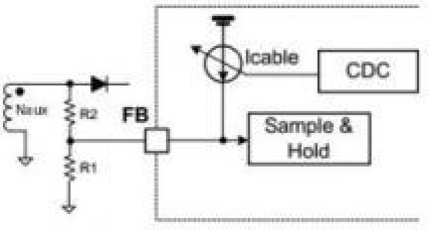
The current magnitude is proportional to the switching period and inversely proportional to the output power Pout. Therefore, the losses caused by cable losses can be compensated. As the load decreases from full load to zero load, the bias voltage of the FB pin will increase.

By adjusting the resistance of R1 and R2 (as shown in the figure), cable voltage drop loss compensation can be programmed. The maximum compensation percentage is given by the following equation:

$$\frac{\Delta V}{V_{OUT}} = \frac{I_{comp\_cable} \times (R1 // R2) \times 10^{-6}}{2.0} \times 100\%$$

eg: R1=3KΩ , R2=18KΩ ,then the maximum compensation is

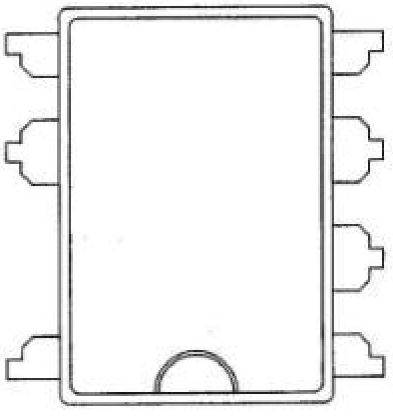
$$\frac{\Delta V(cable)}{Vout} = \frac{60\,\mu A \times (3K//18K)}{2V} \times 100\%$$
$$= 7.7\%$$

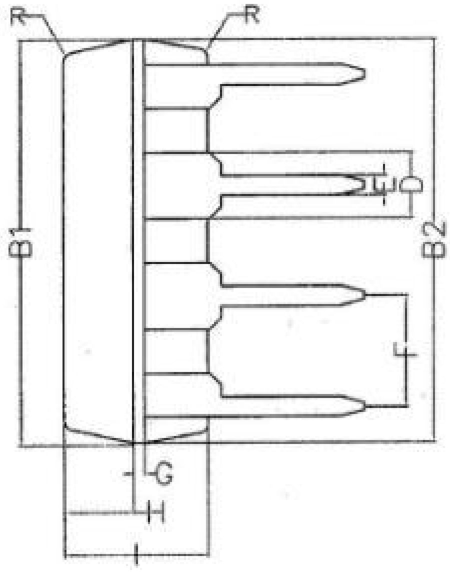


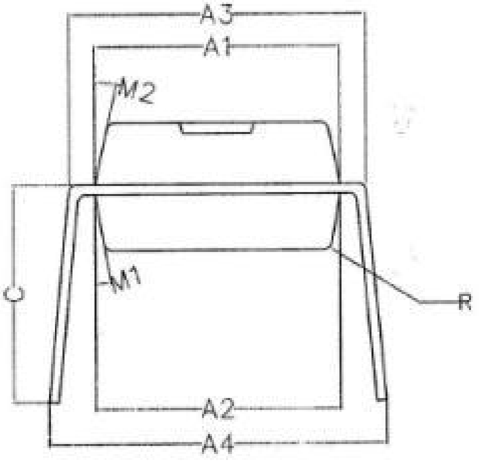
Package Dimensions

DIP-7

(Dimensions in Millimeters)







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9。	10。	11。
M2	11。	12。	13。